AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) An asynchronous data transmitting apparatus, comprising:

a first transmission line having a first delay;

a second transmission line having a delay smaller than the first delay;

a third transmission line having a delay larger than the first delay;

a transmitter that includes

a first transmitting unit that transmits a data signal through the first transmission line, in accordance with a first clock;

a second transmitting unit that transmits a control signal through the second transmission line, in accordance with the first clock; and

a third transmitting unit that transmits the control signal through the third transmission line, in accordance with the first clock; and

a receiver that includes

a clock generator that generates a second clock from the control signals transmitted through the second and third transmission lines, wherein a pulse of the second clock is provided in a period from a first pulse-edge of the control signal transmitted through the third transmission line to a second pulse-edge subsequent to the first pulse edge, the second pulse-edge being of the control signal transmitted through the second transmission line; and

a data receiving unit that receives the data signal through the first transmission line, in accordance with the second clock.

2. (Original) The asynchronous data transmitting apparatus according to claim 1, wherein

the control signal has two binary levels which alternate in each transmission cycle.

3. (Previously Presented) The asynchronous data transmitting apparatus according to claim 1, wherein

the clock generator includes

a first unit that outputs a suppressing signal during a period when logic levels of the control signals do not coincide; and

a second unit that generates the second clock, in response to an end of the suppressing signal, in accordance with a third clock.

4. (Previously Presented) The asynchronous data transmitting apparatus according to claim 3, wherein

the first unit is an EXNOR circuit to which the control signals transmitted through the second and third transmission lines are input, and the EXNOR circuit outputs the suppressing signal, and

the second unit is an AND circuit to which the suppressing signal and the third clock, and the AND circuit outputs the second clock.

5. (Original) The asynchronous data transmitting apparatus according to claim 1, wherein

the control signal is the first clock.

6. (Previously Presented) The asynchronous data transmitting apparatus according to claim 3, wherein

the first unit is a NAND circuit to which the control signal transmitted through the second transmission line and an inversion of the control signal transmitted through the third transmission line are input, and the NAND circuit outputs the suppressing signal, and

the second unit is an AND circuit to which the suppressing signal and the third clock, and the AND circuit outputs the second clock.

7. (Previously Presented) An asynchronous data transmitting apparatus, comprising:

a first transmission line having a first delay;

a second transmission line having a delay smaller than the first delay;

a third transmission line having a delay larger than the first delay;

a transmitter that includes

a first transmitting unit that transmits a data signal through the first transmission line, in accordance with a first clock;

a second transmitting unit that transmits a control signal through the second transmission line, in accordance with the first clock; and

a third transmitting unit that transmits the control signal through the third transmission line, in accordance with the first clock; and

a receiver that includes

a data receiving unit that receives the data signal through the first transmission line, in accordance with a second clock; and

a processing unit that generates an enable signal from the control signals transmitted through the second and third transmission line, and determines whether to read the received data signal based on the enable signal, wherein a pulse of the second clock is provided in a period from a first pulse-edge of the control signal transmitted through the third transmission line to a second pulse-edge subsequent to the first pulse edge, the second pulse-edge being of the control signal transmitted through the second transmission line.

8. (Original) The asynchronous data transmitting apparatus according to claim 7, wherein

the control signal has two binary levels which alternate in each transmission cycle.

9. (Previously Presented) The asynchronous data transmitting apparatus according to claim 7, wherein

the processing unit includes

a first unit that outputs a suppressing signal during a period when logic levels of the control signals do not coincide; and

a second unit that generates the enable signal, in response to an end of the suppressing signal, in accordance with the second clock.

10. (Previously Presented) The asynchronous data transmitting apparatus according to claim 9, wherein

the first unit is an EXNOR circuit to which the control signals transmitted through the second and third transmission lines are input, and the EXNOR circuit outputs the suppressing signal, and

the second unit is a flip flop to which the suppressing signal is input in accordance with the second clock, and the flip flop circuit outputs the enable signal.

11. (Original) The asynchronous data transmitting apparatus according to claim 7, wherein

the control signal is the first clock.

12-20. (Cancelled)